

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte KATHERINE G. HEINEN

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Appeal No. 2000-0158  
Application No. 08/782,872<sup>1</sup>

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ON BRIEF

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Before MARTIN, GROSS, and LEVY, Administrative Patent Judges.  
MARTIN, Administrative Patent Judge.

**DECISION ON APPEAL**

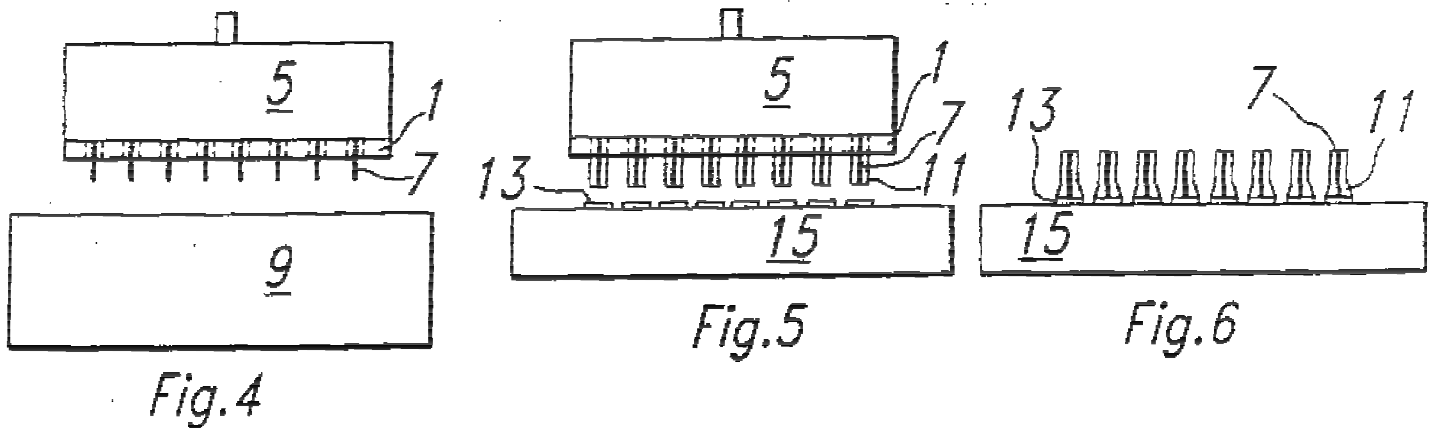
This is an appeal under 35 U.S.C. § 134 from the final rejection of claims 9-16 under 35 U.S.C. § 103(a). Claims 1-8 and 17-19 stand withdrawn by the examiner as directed to a nonelected invention. We reverse and enter a new ground of rejection pursuant to 37 CFR § 1.196(b).

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<sup>1</sup> Application for patent filed January 14, 1997, as a continuation of provisional application No. 60/010,044, filed January 16, 1996.

**A. The invention**

The invention related to the soldering of pins onto an electronic package. As shown in Appellant's Figures 4-6, reproduced below, an electromagnet 5 and an apertured mask 1 are used to pick up magnetic pins 7, dip the pins into a solder bath 9 so as to coat the exposed ends of the pins, and then bring the ends of the pins into contact with solder pads or lands 13 on an electronic package 15, after which heat is applied to cause the solder on the pins to reflow and secure the pins to the package.



**B. The claims**

Claim 9, the sole independent claim on appeal, and dependent claims 10 and 11, read as follows:<sup>2</sup>

9. A partially fabricated package which comprises:

(a) a surface having a plurality of electrically conductive bond pads thereon; and

(b) solder-coated solderable magnetic pins contacting said bond pads, unsecured to said bond pads and solderable to said bond pads.

10. The package of claim 9 wherein said pads are one of solder pads or lands.

11. The package of claim 9 wherein each said solder-coated magnetic pin is secured to said pad by solder coated on said pin.

**C. The references and ground of rejection**

The examiner's rejection is based on the following references:

Ma et al. (Ma)	5,486,723 (US)	Jan. 23, 1996
		(filed Nov. 7, 1994)

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<sup>2</sup> Claim 9 as reproduced herein is claim 9 as it appears in the amendment dated September 3, 1997 (Paper No. 4). We note that the January 23, 1998, amendment (Paper No. 6) to claim 9 has physically been entered despite the examiner's Advisory Action (Paper No. 7) refusing it entry.

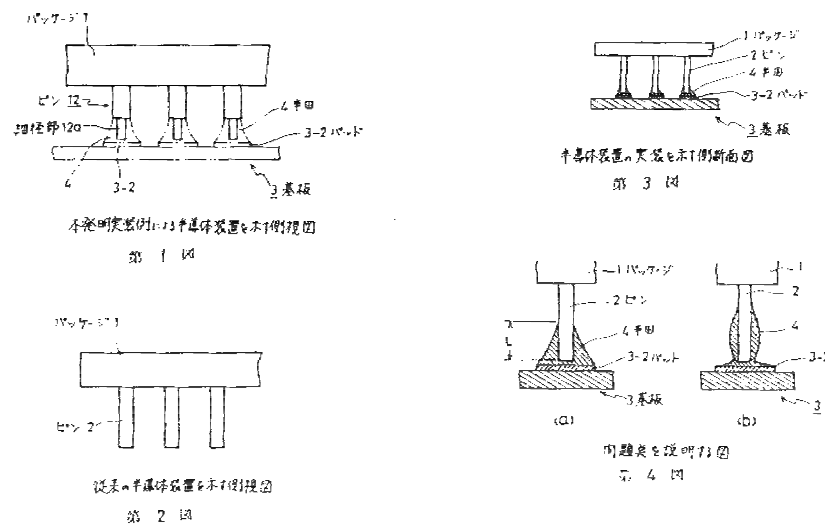
Seyama<sup>3</sup>

64-71159 (JP)

Mar. 16, 1989

Claims 9-16 stand rejected under 35 U.S.C. § 103(a) for obviousness over Seyama in view of Ma.

Figures 1, 3, and 4 of Seyama show pins 2 of semiconductor packages 1 soldered to pads 3-2 on substrates 3:

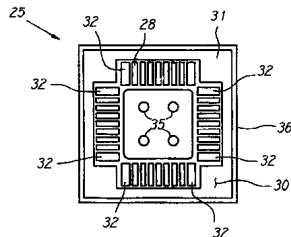


Before the pins' ends are brought into abutting contact with the pads, the solder is applied to the substrate rather than being applied to the pins, as is necessary to satisfy claim 1.

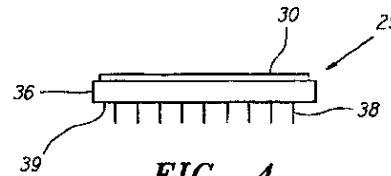
Translation at 5, 3rd full para.

<sup>3</sup> Our understanding of this reference is based on the November 1, 1999, translation prepared by the PTO Translations Branch (copy enclosed).

The examiner attempts to cure this deficiency by relying on Ma's disclosed techniques for soldering pins 38 and 80 to an add-on card 25 (Answer at 4). We will begin with pins 38 (Fig. 4), which extend from the bottom surface of add-on card 25, the top, bonding surface 30 (Fig. 3) of which has pads 28 and 32 for soldering to leads 22 of a plastic quad flat pack (not shown).

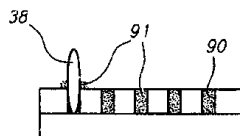


**FIG. 3**

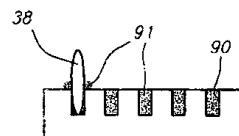


**FIG. 4**

Figs. 19 and 20 show the pins 38 mounted in holes 90 of embodiments of add-on card boards having single-layer and double-layer construction:



**FIG. 19**



**FIG. 20**

Ma does not coat the pins with solder before inserting them into holes 90. Instead,

[s]older paste 91 is . . . placed in holes 90. After applying the solder paste to the holes 90, preferably filling them completely, the pins 38 are inserted. The

add-on card 25 with the pins 38 inserted is then heated. This heating process melts the solder surrounding the base of the pin.

Ma, column 8, lines 35-39. The pins are connected to soldering pads 28 (Fig. 3) by unshown circuitry between the board layers and on the bonding surface 30 of the add-on card (col. 8, ll. 41-43).

Nor are the heads 82 of Ma's pins 80 (Fig. 13) coated with solder before being secured to pin pads 84 on add-on card 25's board 36 (Fig. 15):

(Fig. 3)

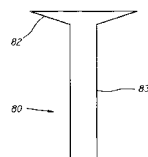


FIG. 13

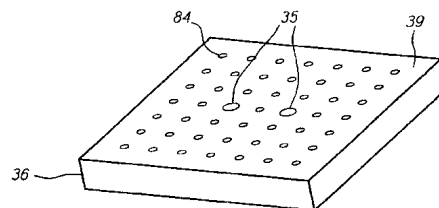


FIG. 15

Instead, Ma explains that

[u]sing a stencil matching the pin layout of the PGA socket, a thin layer of solder paste is disposed on the pin pads 84. The fixture containing the pins 80 is then placed on the add-on card 25. . . .

Once the fixture is placed on the add-on card 25, the assembly is placed in a reflow oven (not shown) that melts the solder, thereby securing the pins 82 to the add-on card 25.

Ma, column 8, line 67 to column 9, line 14.

Inasmuch as neither reference discloses coating the pins with solder prior to bringing them into contact with the pads, we cannot sustain the § 103 rejection of any of claims 9-16.

**D. New ground or rejection pursuant to 37 CFR § 1.196(b)**

Claims 11 and 12 and their dependent claims 15 and 16 are hereby rejected under 35 U.S.C. § 112, fourth paragraph, for failing to further restrict claim 9, on which claim 11 depends directly and claim 12 depends indirectly through claim 10. Specifically, whereas claim 9 recites that the pins are "unsecured" to the bond pads and "solderable thereto," claims 11 and 12 specify that each of the pins "is secured to said bond pad by solder coated on said pin." Consequently, it is possible to infringe claims 11 and 12 without infringing claim 9, which violates the "infringement test" for proper claim dependency discussed in MPEP § 608.01(n) at page 600-77 (8th ed. Aug. 2001), Ex parte Porter, 25 USPQ2d 1144, 1147 (Bd. Pat. App. & Int. 1992), and Ex parte Moelands, 3 USPQ2d 1474, 1476 (Bd. Pat. App. & Int. 1987).

**E. Appellant's options for responding to new ground of rejection**

This decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b) (amended effective Dec. 1, 1997, by final rule

notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides, "[a] new ground of rejection shall not be considered final for purposes of judicial review."

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

(1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the application will be remanded to the examiner . . . .

(2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record . . . .



Appeal No. 2000-0158  
Application No. 08/782,872

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

**REVERSED; 37 CFR § 1.196(b)**

JOHN C. MARTIN	)	
Administrative Patent Judge	)	
	)	
	)	
	)	BOARD OF PATENT
ANITA PELLMAN GROSS	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
STUART S. LEVY	)	
Administrative Patent Judge	)	

JCM/sld

Appeal No. 2000-0158  
Application No. 08/782,872

CC:

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Enclosure: PTO translation of Seyama.